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# ELECTRONIC COMPONENT ALLOWING THE DECODING OF DIGITAL TERRESTRIAL OR CABLE TELEVISION SIGNALS

## PRIORITY CLAIM

[1] The present application claims priority from French Application for Patent No. 03 04138 filed April 3, 2003, the disclosure of which is hereby incorporated by reference.

## BACKGROUND OF THE INVENTION

### Technical Field of the Invention

[2] The present invention relates to the decoding of radiofrequency transmission channels conveying coded digital information.

[3] The invention thus applies advantageously to digital terrestrial television, that is to say using signals transmitted between television antennas, as defined, for example, in the European DVB-T (Digital Video Broadcasting - Terrestrial) specification, or to digital cable

television, as defined, for example, in the European DVB-C (Digital Video Broadcasting - Cable) specification, all these telebroadcasts being based on the MPEG transmission standards, and use for example to convey information, quadrature digital modulation, or modulation of the COFDM type according to terminology well known to the person skilled in the art. The invention thus relates in particular to tuners, and also to demodulators and to the actual processing for channel decoding.

Description of Related Art

[4] The television signals received at the input of the tuner of the receiver are composed of the entire set of transmitted channels that lie in the 50 MHz-850 MHz frequency band.

[5] The objective of the tuner is to select the desired channel and to output a baseband signal on the in-phase path (I path) and on the quadrature path (Q path). This signal is thereafter converted into a digital signal and demodulated. The channel decoding processing thereafter also comprises a block which distinguishes, typically by means of majority logic, zeros from ones, then performs all the error correction, that is to say typically a Viterbi decoding, deinterleaving, Reed-Solomon decoding and deshuffling. The channel decoding device outputs packets that are decoded in a conventional manner in a source decoding device in accordance with the MPEG standards so as to regenerate the initial audio and video signals transmitted via antennas or via the cable.

[6] Current studies are aimed at researching ever more integrated solutions for embodying digital terrestrial or cable receivers. However, this research is confronted by technological difficulties related to the embodying of the means making it possible, on the one

hand, to correctly discern a channel from the entire set of channels present, and, on the other hand, to correctly discriminate the signal from noise.

[7] Specifically, whereas in digital satellite television, all the channels have nearly the same power, this is not the case in particular in digital terrestrial television. Thus, it is for example possible to have adjacent channels exhibiting a very high power with respect to the desired channel, for example a difference in power of the order of 35 dB. It is therefore necessary to be able to ensure a rejection of 35 dB on the adjacent channels. Moreover, the specification imposes a signal/noise ratio of the order of 35 dB. Hence, in the worst case, it is therefore essential for it to be possible to bring the level of an adjacent channel to 70 dB below its input level.

[8] This results in extremely significant constraints on the filters, this being extremely constraining in respect of integrated solutions. The invention aims to afford a solution to this problem. There is a need in the art to present a solution offering maximum integration, given the characteristics of digital television signals, in particular terrestrial ones, exhibiting more significant rejection constraints than digital cable television signals.

## SUMMARY OF THE INVENTION

[9] The invention therefore proposes an electronic component comprising

a tuning module, or tuner, of the zero intermediate frequency dual conversion, upconversion then downconversion, type, possessing an input able to receive digital terrestrial or cable television analog signals composed of several channels, a bandpass filter of the surface acoustic wave type disposed between the two frequency transposition stages of the tuning

module, and delivering a filtered analog signal containing the information conveyed by a desired channel and so-called "adjacent channel" information, a baseband filtering stage disposed on the two quadrature output paths of the second frequency transposition stage for performing a first filtering of the adjacent channel information,

a multibit analog/digital conversion stage linked to the output of the baseband filtering stage,

a digital block comprising a stage for correcting the defects of phase- and amplitude-pairing of the two processing paths, and a channel decoding digital module linked to the output of the defect correcting stage, this digital decoding module comprising a demodulation stage, a digital filtering stage for eliminating the said adjacent channel information, and an error correcting stage for delivering a stream of data packets corresponding to the information conveyed by the desired channel.

[10] Moreover, with the exception of the surface acoustic wave filter, the tuning module, the analog/digital conversion stage and the digital block are disposed within an integrated circuit embodied on a monolithic substrate.

[11] Stated otherwise, the invention solves in particular the problem of the filtering of the adjacent channels by using in combination, an external filter of the surface acoustic wave type (SAW filter), an integrated baseband filter, and a digital filter. Thus, the surface acoustic wave filter, which is by nature a relatively steep filter, performs a prefiltering of the signal so as to allow through only the desired channel and a few adjacent channels. Then, the elimination of the adjacent channels proceeds with the baseband analog filter which is a relatively soft filter,

and terminates with the digital filter (Nyquist filter) at the output of which the adjacent channel information is eliminated.

[12] Moreover, the multibit resolution of the analog/digital conversion stage, for example at least equal to four bits, allows sufficient accuracy to be obtained ultimately, with regard to the information of the desired channel.

[13] Thus, the distribution of the adjacent channel filtering function according to the invention helps to allow the embodying, on one and the same chip, of all the components of the receiver, and to retain only the surface acoustic wave filter as external component.

[14] According to one embodiment of the invention, the first frequency transposition stage is able to receive a first transposition signal having a frequency equal for example to the sum of the frequency of the desired channel and of a first transposition frequency greater than the upper limit of the said frequency span. It will be possible to choose for example a first transposition frequency equal to 1220 MHz.

[15] This said, it could also be possible for the frequency of the transposition signal to be equal to the difference between the first transposition frequency and the frequency of the desired channel.

[16] Choosing a first transposition frequency greater than the upper limit of the frequency span, that is to say greater than 850 MHz, makes it possible to proceed with this upconversion, outside the receive band, and thus to avoid interactions with the first transposition frequency.

[17] Moreover, the second frequency transposition stage, that is to say the one that will bring the signal back to baseband, is able to receive a second transposition signal having the said first transposition frequency, that is to say in this instance 1220 MHz.

[18] The passband of the surface acoustic wave filter is for example of the order of two to three times the frequency width of a channel. Thus, by way of indication, the frequency width of a channel being of the order of 8 MHz, it will be possible to choose a passband of the order of 20 MHz for the surface acoustic wave filter.

[19] For its part, the bandpass filtering stage possesses an upper cutoff frequency of around 20% greater than the frequency half-width of a channel.

[20] Moreover, although the sampling frequency of the analog/digital conversion stage is advantageously greater than around 2.5 times the upper cutoff frequency of the baseband filtering stage, it is particularly advantageous to provide a much higher sampling frequency, for example of the order of some 100 MHz and more generally at least ten times greater than the upper cutoff frequency of the baseband filtering stage, so as to perform an oversampling of the signal. Thus, this oversampling, in combination with a multibit resolution, makes it possible, in particular when a decimater filter is disposed downstream of the analog/digital converter, to extract the desired channel with a multibit resolution, and hence to be able to correctly utilize the information contained in this desired channel.

[21] According to one embodiment of the invention, the cutoff frequency of the digital filtering stage is equal to the frequency half-width of a channel.

[22] According to one embodiment of the invention, the component comprises a metal plate glued to the rear surface of the substrate by a conducting glue, this metal plate being

intended to be grounded. Thus, the capacitance, of relatively high value, produced between the semiconductor substrate and the metal plate, makes it possible to absorb the high-frequency current spikes.

[23] Moreover, it is particularly advantageous for the elements performing a digital processing to be disposed in a part of the substrate that is isolated from the remaining part of the substrate by a semiconducting barrier having a type of conductivity different from the type of conductivity of the substrate. Stated otherwise, a so-called "triple well" technology is used. This makes it possible, when the semiconducting barrier is biased by a bias voltage different from that supplying the transistors situated in the isolated part of the substrate, to prevent noise on the supply voltage of the transistors from being transmitted directly via the substrate to the various analog components of the receiver.

[24] The subject of the invention is also a terrestrial or cable digital television signal receiver, comprising an electronic component as defined hereinabove.

## BRIEF DESCRIPTION OF THE DRAWINGS

[25] A more complete understanding of the method and apparatus of the present invention may be acquired by reference to the following Detailed Description when taken in conjunction with the accompanying Drawings wherein:

[26] FIGURE 1 is a schematic of the internal structure of an electronic component according to the invention;

[27] FIGURE 2 diagrammatically illustrates s frequency chart of channels before and after filtering;

[28] FIGURE 3 diagrammatically illustrates s frequency chart of channels before and after filtering;

[29] FIGURE 4 diagrammatically illustrates in greater detail the internal structure of a channel decoding module of a component according to the invention; and

[30] FIGURE 5 diagrammatically illustrates a technological embodiment of a component according to the invention.

DETAILED DESCRIPTION OF THE DRAWINGS

[31] In FIGURE 1, the reference RDS denotes a receiver/decoder connected to a antenna ANT picking up digital terrestrial television signals, this receiver being intended to receive and to decode these signals. The receiver RDS comprises at the head end an electronic component CMP intended to receive all the channels $CN_i$ present in the signal received at the signal input ESO of this component, and to deliver, at the output BSO, an MPEG data stream corresponding to a selected channel.

[32] The component CMP comprises an integrated circuit IC (chip) embodied entirely in CMOS technology on a monolithic silicon substrate. The component CMP comprises at the head end a tuning device or "tuner" TZ, intended for selecting a channel from all the channels $CN_i$ present in the signal received at the signal input ESO, which here is also the input of the tuner. This tuner TZ is here a dual-conversion tuner, first upconversion then downconversion with zero intermediate frequency, so as to ultimately bring the signal back to baseband. More precisely, the tuner TZ comprises an analog block BAN, separated from a digital block BNM by

an analog/digital conversion stage CANI and CANQ. The analog block BAN, the digital block BNM and the analog/digital conversion stage CANI and CANQ are embodied on the chip IC.

[33] The tuner TZ comprises at the head end a low noise amplifier LNA connected to the signal input ESO. This amplifier LNA is followed by a first frequency transposition stage (mixer) MX1. This mixer MX1 receives, on the one hand, the signal emanating from the low noise amplifier LNA and, on the other hand, a transposition signal OL1 emanating for example from a voltage-controlled oscillator VCO1. This transposition signal OL1 has a frequency equal to the sum of the frequency Fd of the desired channel and of a first transposition frequency which is chosen to be greater than the upper limit of the 50 MHz-850 MHz frequency span. By way of example, a frequency equal to 1220 MHz may be chosen as first transposition frequency. Consequently, the signal at the output of the mixer MX1 is, as illustrated in FIGURE 2, a signal comprising all the channels, but whose desired channel $CN_i$ is centered around the first transposition frequency, that is to say 1220 MHz.

[34] One then proceeds to a first bandpass filtering of the signal emanating from the mixer MX1 in an external filter of the surface acoustic wave type FSAW. This filter is external, in the sense that it is situated outside the integrated circuit IC. Filters of the surface acoustic wave type are known per se to the person skilled in the art. It will, for example, here be possible to use a filter exhibiting a center frequency of 1220 MHz, such as that marketed by the German company EPCOS AG, under the reference B 1610. This filter FSAW is by nature relatively steep and consequently makes it possible to eliminate a large number of undesired adjacent channels situated on either side of the desired channel $CN_i$. By way of indication, the EPCOS B 1610 filter exhibits a passpand of 20 MHz. Given the fact that the width of a channel is of the

order of 8 MHz, the output signal from the filter FSAW will comprise the desired channel CNi and two or three immediately adjacent channels, as is also illustrated diagrammatically in FIGURE 2.

[35] On output from the filter FSAW, the signal is amplified in a controlled-gain amplifier AGC. Then, this signal undergoes a second conversion, this time a downconversion, within a second frequency transposition stage here formed of two mixers MX2I and MX2Q, respectively receiving two frequency transposition signals OL2 mutually out of phase by 90°. These frequency transposition signals OL2 emanate for example also from a voltage-controlled oscillator VCO2. The frequency of the second transposition signal OL2 is equal to the first transposition frequency, that is to say here 1220 MHz. The second frequency transposition is therefore here of the type with zero intermediate frequency since it will bring the signal directly back to baseband. Stated otherwise, two baseband quadrature analog signals, that is to say ones exhibiting the desired channel centered around the zero frequency, are obtained at the output of the two mixers MX2I and MX2Q, on the two processing paths I and Q.

[36] In the subsequent text, only one of the two processing paths will now be described, for example the I path, it being understood of course that the Q path exhibits an analogous structure.

[37] At the output of the mixer MX2I is disposed an analog filter FBBI whose template has been diagrammatically represented in FIGURE 3. In this figure, the reference F1, equal to 6 MHz, represents the frequency half-width of the channel $CN_i$. The person skilled in the art is aware that this frequency half-width in fact corresponds to the theoretical frequency

half-width of a channel (for example 4 MHz) multiplied by a coefficient known as "roll off", and which is for example equal to 1.35.

[38] The baseband filter FBBI has an upper cutoff frequency equal to F2. According to the invention, this frequency F2 is chosen to be at least 20% greater than the frequency half-width F1 of the channel $CN_i$. By way of indication, it will for example be possible to choose an upper cutoff frequency F2 of each baseband filter FBB equal to around 8 MHz. Thus, a filtered signal comprising the information ICN conveyed by the selected channel, and so-called "adjacent channel residual information" IACD are obtained at the output of these two baseband filters FBBI and FBBQ.

[39] The person skilled in the art will consequently have appreciated that this analog filter, which is for example a filter of order 6, is a relatively soft filter, in the sense that it allows through adjacent channel information. However, the use of a soft analog filter allows easy integration thereof on silicon.

[40] The analog signals at the output of the filters FBBI and FBBQ are digitized in analog/digital converters CANI and CANQ, which exhibit for example here a sampling frequency of the order of 100 MHz with a resolution of the order of 14 bits.

[41] The internal structure of the digital block BNM will now be described in greater detail. In addition to the control means CTL, which may for example be embodied in software form within a microcontroller, and are intended to control the amplifier AGC, the block BNM comprises at the head end correction means MCOR intended to correct defects of phase- and amplitude-pairing of the two processing paths I and Q. Such correction means are known per se

to the person skilled in the art. The latter may refer, for whatever purpose it may serve, to US patent No. 6,044,112, or to French Patent Application No. 02 03256 in the name of the applicant.

[42] The digital block BNM next comprises a channel decoding module DM, an example of the structure of which is illustrated more particularly in FIGURE 4. More precisely, this channel decoding digital module DM comprises a demodulation stage DMD capable of performing conventional demodulation processing, followed by an error correction stage CRE performing conventional Viterbi decoding processing, deinterleaving, Reed-Solomon decoding deshuffling, so as to deliver the packet FM that will be decoded in a source decoding block external to the component CMP, and in accordance with the MPEG standard for example.

[43] The demodulation stage DMD diagrammatically comprises at the head end correction means DRT (Derotator) able to correct the phase noise, the frequency drift and the frequency offset of the frequency synthesizers. The correction means DRT are also used here according to the invention to compensate for the bandpass filtering FBBI, FBBQ and thus avoid obtaining too low an error margin for the interpretation of the constellation. Such means of derotation may for example be those described in European Patent Application No. 0,481,543.

[44] The analog filtering is here supplemented with Nyquist filtering performed in a digital filter FN, whose cutoff frequency is equal to the frequency half-width F1 of the desired channel. The filter FN consequently supplements the filtering performed by the filter FSAW and the bandpass filter FBBI, FBBQ, and thus eliminates the adjacent channel information.

[45] The error correction stage CRE next performs conventional error correction processing that is well known to the person skilled in the art by the terminology FEC (Forward Error Correction).

[46] Technologically, the integrated circuit IC according to the invention is embodied, for example in 0.18 μm CMO technology, on a monolithic substrate SB made of silicon, for example of $P^-$ type (FIGURE 5). To absorb the high-frequency current spikes, it is preferable to glue a metal plate PL onto the rear face of the substrate SB by means of a conventional conducting glue CL. This metal plate is intended to be grounded. The fine layer of oxide which forms naturally on the silicon of the substrate forms the dielectric of a capacitor whose two electrodes are formed respectively by the substrate SB and the metal plate PL. This capacitor, whose capacitance is relatively large, thus makes it possible to absorb the high-frequency current spikes.

[47] Moreover, the digital part of the component CMP, that is to say in this instance the digital block BNM, is made in a region ZN of the substrate which is isolated from the remainder of the substrate (in which region the analog part BAN of the component is made) by an $N^-$ -doped semiconducting barrier formed here of a buried layer CH1 and two wells PT1 and PT2.

[48] Moreover, the PMOS transistors of the digital part are made within an $N^-$ well which comes into contact with the buried layer CH1.

[49] Also, in order to prevent the noise on the supply voltage Vdd from being transmitted via the $N^-$ wells to the analog part, so that it directly disturbs in particular the amplifier LNA, it is advantageous to bias all the $N^-$ wells with a bias voltage different from that supplying the transistors situated in this isolated region ZN of the substrate.

[50] Although preferred embodiments of the method and apparatus of the present invention have been illustrated in the accompanying Drawings and described in the foregoing

Detailed Description, it will be understood that the invention is not limited to the embodiments disclosed, but is capable of numerous rearrangements, modifications and substitutions without departing from the spirit of the invention as set forth and defined by the following claims.